



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Hsuan, John)	Art Unit: 2811
Serial No.: 10/634,404)	Examiner: Unassigned
Filed: August 5, 2003 as a divisional of serial number 10/167,118, filed June 11, 2002, which is a continuation of serial number 09/304,244, now U.S. patent 6,429,509)))	
For: Intermediate structure for making integrated circuit device & wafer		

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313

Sir:

- 1. Pursuant to 37 C.F.R. 1.97 and 1.98, and in compliance with 37 C.F.R. 1.56, the Office's attention is directed to the patents, publications and other information listed on the attached PTO-1449. Regarding the document(s), publication(s) or other information listed on the attached PTO-1449, Applicant believes the same may qualify as "prior" art to this application and should be treated accordingly, although Applicant(s) reserve(s) the right to contest the prior art status of any document, publication or information cited herein.
- 2. Pursuant to 37 C.F.R. 1.97(b) this Statement is being filed within 3 months of the filing date.
- 3. Copies of the aforementioned references were provided in the parent application to the above by the Applicant and/or cited by the examiner. Should it be necessary for the applicant to provide additional copies, please contact the undersigned.

Attorney Docket No.: UMC99-001D2

Respectfully submitted,

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I hereby certify that the foregoing is being deposited with the U.S. Postal Service, postage prepaid, to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313, this 4th day of November 2003



Information Disclosure Statement By Applicant Substitute for form 1449/PTO

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Application Number: 10/634,404

Filing Date: 08/05/2003 First Named Inventor: Hsuan

Art Unit: 2811 Examiner Name: N/A

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Examiner	Date
Signature:	Considered: